

The *fun* Instruction-set Architecture Manual  
v.0.1

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# Chapter 1

## About this Manual

*fun* is a purely-functional instruction set architecture that defines a language based on structured combinators, for applications where isolation, purity and the way computation is actually performed are the central concerns.

This is the first draft of a document that describes the *fun* instruction-set architecture (ISA). This manual does not describe any implementation-specific details such as reduction model, evaluation order or hardware structures such as registers, caches, memories, bus interfaces, garbage collectors and other memory management units.

This document is open to contributions from anyone interested to participate in the *fun* project, and as such, it is a *wok in progress*. The information contained in this manual may change as the architecture and its implementations evolve.

Other relevant material about *fun* should be also available on the project wiki, at <http://wiki.fun-arch.org>.

If you wish to contribute on this manual or the wiki, send a request to the email [join@fun-arch.org](mailto:join@fun-arch.org).

## Chapter 2

# Introduction

### 2.1 Features

*fun* is a purely-functional instruction set architecture that defines a language based on structured combinators, for applications where isolation, purity and the way computation is actually performed are the central concerns. *fun* is:

- An open, free and community-driven instruction-set architecture;
- The first purely-functional instruction set based on combinators to follow a modern, proven path of other RISC architectures;
- A purely-functional instruction set for which memory handling, control flow and other stateful and effectful behaviors is *unrepresentable*.
- An instruction set for efficient implementation of high-level purely-functional programming languages.

## Chapter 3

# A Timeline of Functional Programming and Machine-Support for Functional Programming

### 3.1 Foundations

- 1924 – M.Schonfinkel: Uber die Bausteine der Mathematischen Logik
- 1930 – H.B.Curry: Grundlagen der Kombinatorischen Logik
- 1934 – H.B.Curry: Functionality in Combinatory Logic
- 1958 – H.B.Curry, R.Feys: Combinatory Logic (Book)

### 3.2 Technology Trigger

- 1971 – C.P.Wadsworth: Semantics and Pragmatics of the  $\lambda$ -calculus
- 1977 – J.Backus: Can Programming Be Liberated from the von Neumann Style? A Functional Style and Its Algebra of Programs
- 1979 – D.Turner: A new Implementation Technique for Applicative Languages
- 1979 – D.Turner: Another Algorithm for Bracket Abstraction
- 1982 – D.Turner: Miranda

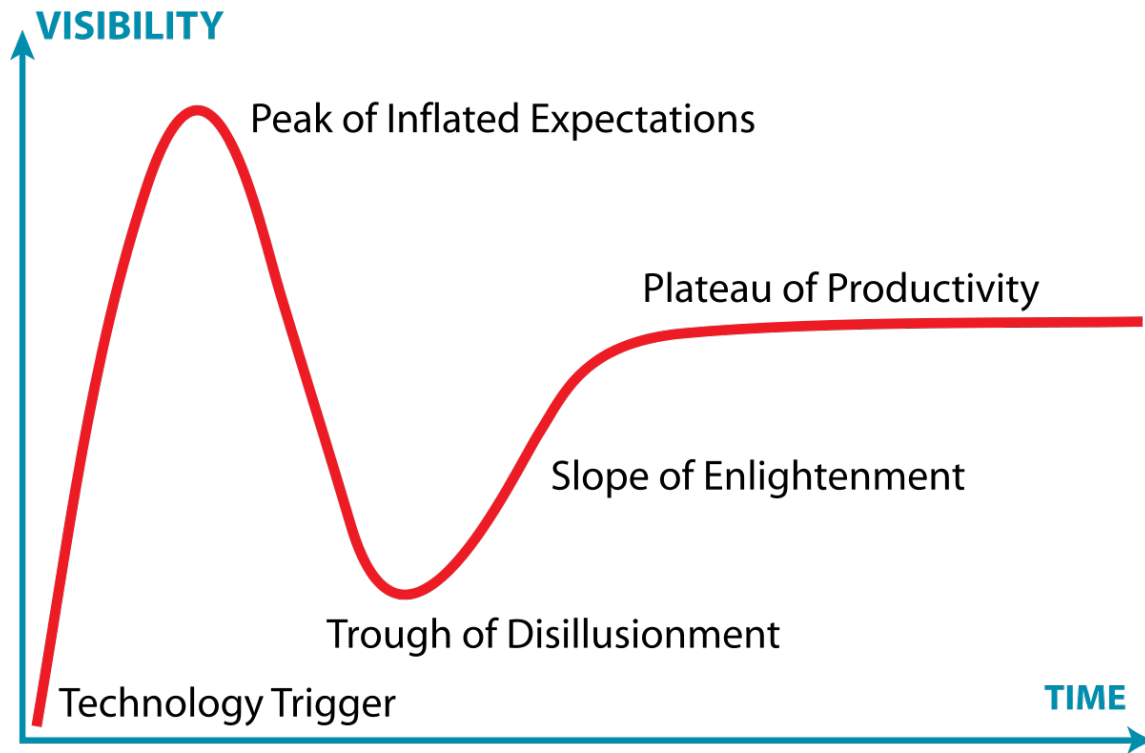


Figure 3.1: Hype cycle

### 3.3 Peak of Inflated Expectations

#### LISP Machines

#### Combinator Architectures

- 1980 – T.J.W.Clarke: SKIM – The S, K, I Reduction Machine
- 1984 – W.R.Stoye: Some Practical Methods for Rapid Combinator Reduction
- 1985 – W.Stoye: Message-based Functional Operating Systems
- 1986 – M.Scheevel: NORMA, A Graph Reduction Processor
- 1986 – J.Ramsdell: The CURRY chip
- 1990 – P.J.Koopman: Implementation of the TIGRE Machine

## Parallel & Dataflow

- 197? – Arvind: Dataflow
- 1986 – C.Clack, SPJ: The Four-stroke Reduction Engine
- 1988 – SPJ,et al: GRIP

## 3.4 Disillusionment

### Functional Programming in Stock Hardware

- 1982 – J.Hughes: Supercombinators- A new implementation method for applicative languages
- 1984 – G-Machine
- 1987 – Spineless Tagless G-machine
- 1987 – Haskell

## 3.5 Enlightenment

- Category Theory: Morphisms
- Haskell, OCaml, Erlang, Elm: real-world functional programming languages
- Mainstream FP: Immutable data, higher-order functions on Python, JavaScript, Java, C++
- Industrial use of FP: Specification, theorem proofing, finance, safety

## 3.6 Reattempts

- 2007 – Naylor: Reduceron
- 2010 – Naylor: Reduceron Reconfigured
- 2017 – McMahan: An Architecture Supporting Formal and Compositional Binary Analysis (Zarf)
- 2020 – Pope: Cephalopode
- 2020 – Coelho: ACQuA



## Chapter 4

# Combinator Graph Reduction

This chapter is a stub for a discussion on Combinator Graph Reduction.

## Chapter 5

# Instruction Formats

This chapter describes the instruction encoding of the *fun* ISA, its formats and types.

*fun* instructions are divided into 4 types (C/ $I^2$ /A/V), as depicted in Fig.5.1. Each instruction fits a 36-bit word, with a 4-bit *tag*, and a 36-bit *payload*. Each *tag* is composed by an *eval bit* EV and a type identifier (OP/LIT/LINK/HLINK/ROOT). Table5.1 lists the base types for *fun*, as of version 0.1.

A *fun* instruction can be seen as a graph node for evaluation following a graph reduction strategy.

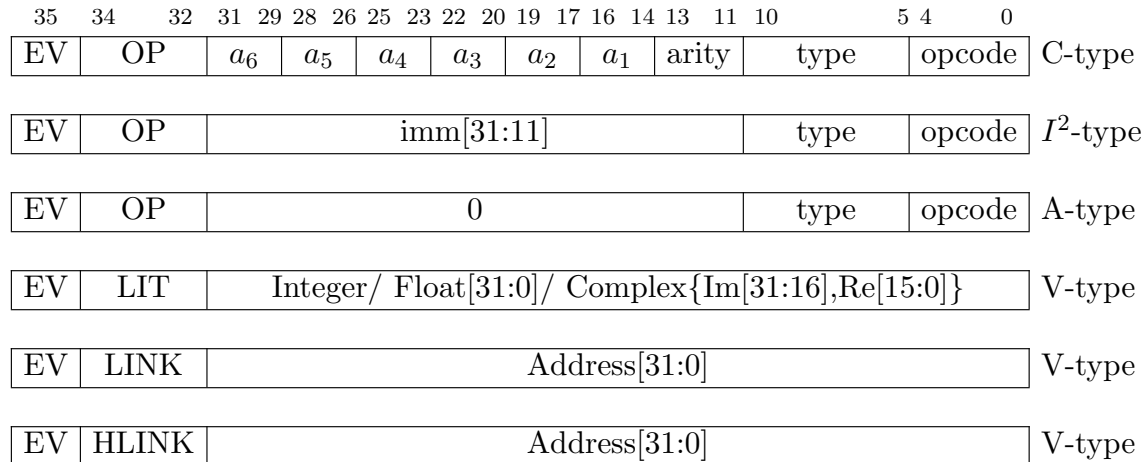


Figure 5.1: Instruction formats for Fun, extended with RISC-V base instructions. A tag[34:32] indicates the type of the instruction.

Type LINK and HLINK identify references to other nodes or strings of combinators.

Table 5.1: Basic types

<b>Type</b>	<b>Encoding</b>
LINK	011
HLINK	110
LIT	001
OP	010
ROOT	111

Type **LINK** is reserved for references made a compile time, by a programmer or compiler, for references to other nodes on the program graph (subgraphs, functions or bus locations).

Type **HLINK** is reserved for references made on runtime by a *fun* CPU, and should not be declared on the initial program graph.

Type **OP** is reserved for *combinators* and other operations for integer arithmetic, floating-point arithmetic, bitwise boolean logic, input-output, and other types defined in the base ISA specification.

Type **LIT** is reserved for pure integer or single-precision floating-point values.

Type **ROOT** is reserved to identify the root node of a program graph.

## Chapter 6

# Combinators

Combinators are instructions of type C that operate on the program graph changing its structure, following the rules specified in the instruction body.

A reduction rule is specified by the *reduction pattern*, *arity* and the contents of each new graph node after reduction.

The base specification for *fun* supports up to 64 reduction patterns, listed on Appendix A.

35	34	32	31	0	34	32	34	32	34	32	34	32	34	32	34	32	10	5	4	0
ev	type	a6	a5	a4	a3	a2	a1	arity	pattern	opcode										
1	3	3	3	3	3	3	3	3	6	5										
EV	OP	a6	a5	a4	a3	a2	a1	num	T0-T63	COMBI										

## Chapter 7

# Integer Instructions

This chapter is a stub for a detailed description of the instructions for integer arithmetic and logic of the *fun* ISA.

## Chapter 8

# Floating-Point Instructions

This chapter is a stub for a detailed description of the instructions for floating-point arithmetic of the *fun* ISA.

## Chapter 9

# Input-Output

This chapter is a stub for a detailed description of the instructions and mechanisms for I/O in *fun* .

## Chapter 10

# Floating-Point Instructions

This chapter is a stub for a detailed description of the instructions for floating-point arithmetic of the *fun* ISA.



## Chapter 11

# Instruction Listings

The listing for the base set of *fun* instructions is shown on Table [11.1](#).

		35	34	32	31	29	28	26	25	23	22	20	19	17	16	14	13	11	10		5	4	0	
EV	OP	$a_6$	$a_5$	$a_4$	$a_3$	$a_2$	$a_1$	arity	type	opcode	C-type													
EV	OP	imm[31:11]								type	opcode	$I^2$ -type												
EV	OP	0								type	opcode	A-type												

### Base Instruction Set

EV	OP	$a_6$	$a_5$	$a_4$	$a_3$	$a_2$	$a_1$	arity	type	11000	combi		
EV	010	0									000000	10001	add
EV	010	0									000001	10001	sub
EV	010	0									000011	10001	sll
EV	010	0									000111	10001	srl
EV	010	0									001000	10001	sra
EV	010	0									001011	10001	mul
EV	010	0									001111	10001	div
EV	010	0									010001	10001	rem
EV	010	0									010101	10001	eq
EV	010	0									010110	10001	gt
EV	010	0									010111	10001	lt
EV	010	0									001010	10001	and
EV	010	0									001011	10001	or
EV	010	0									001100	10001	xor
EV	010	imm[31:11]									000000	10011	addi
EV	010	imm[31:11]									000011	10011	slli
EV	010	imm[31:11]									000111	10011	srlr
EV	010	imm[31:11]									001000	10011	srair
EV	010	imm[31:11]									001011	10011	mulr
EV	010	imm[31:11]									001111	10011	divr
EV	010	imm[31:11]									010001	10011	remr
EV	010	imm[31:11]									010101	10011	eqr
EV	010	imm[31:11]									010110	10011	gtr
EV	010	imm[31:11]									010111	10011	ltr
EV	010	imm[31:11]									001010	10011	andir
EV	010	imm[31:11]									001011	10011	orir
EV	010	imm[31:11]									001100	10011	xorir
EV	010	0									000001	11110	fix
EV	010	0									000100	11110	seq
EV	010	0									010000	11110	out
EV	010	0									001010	11110	break

Table 11.1: Instruction listing for *fun*

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